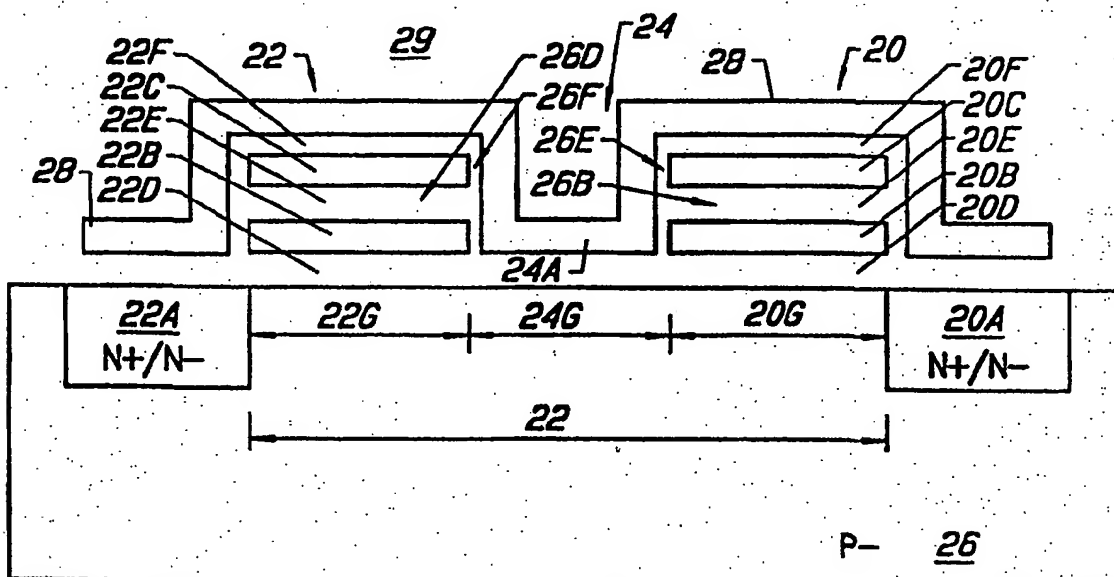




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(54) Title: A SELF-ALIGNED DUAL-BIT SPLIT GATE (DSG) FLASH EEPROM CELL

**(57) Abstract**

An EEPROM cell structure includes two floating gate transistors (20, 22) separated by a select gate transistor (24) with the select transistor being shared by the two floating gate transistors in programming, reading, and erasing a floating gate transistor. The floating gates (20B, 22B) of the two transistors are formed from a first polysilicon layer, the control gates (20C, 22C) of the two transistors are formed from a second polysilicon layer, and the select gate (24A) is formed from a third polysilicon layer. The channel length (24G) of the select transistor is fully self-aligned to the floating gate transistors (20, 22). A word line (28) is formed over the control gates and forms the select gate. The word line (28) runs generally perpendicular to bit lines (22A, 20A) which contact the drain regions of the two floating gate transistors. Accordingly, a virtual ground flash EEPROM memory array can be fabricated using the EEPROM cell structure.

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A SELF-ALIGNED DUAL-BIT SPLIT GATE (DSG) FLASH EEPROM CELLBACKGROUND OF THE INVENTION

This invention is related to our co-pending application serial no. 07/585,811 filed September 20, 1990 for "Triple Polysilicon Flash Eprom Device."

5 This invention relates generally to semiconductor memory devices, and more particularly the invention relates to a triple polysilicon self-aligned split gate flash EEPROM cell.

10 A 5 volt only triple-poly flash EEPROM cell with a split gate structure is disclosed in Naruke, et al., "A New Flash-Erase EEPROM Cell With a Sidewall Select-Gate On Its Source Side," Technical Digest of IEEE Electron Device Meeting 1988. As disclosed therein, a double polysilicon floating gate transistor is formed by
15 first and second layers of polysilicon using conventional processing, and a select gate transistor is then formed by using an etching-back technology after depositing a third layer of polysilicon. The length of the select gate transistor is defined by the height of the double
20 polysilicon floating gate transistor which is about 0.4 um. Due to the etching-back technology, the select gate transistor must run parallel to the control gate.

FIG. 1 illustrates the disclosed flash EEPROM cell. The flash EEPROM cell comprises N+ source region
25 11a and N+/N- drain region 11b separated by channel region 12. Channel region 12 consists of a portion 12a beneath the floating gate 13 and a portion 12b beneath the select gate 14. Overlying channel region 12 is gate dielectric 16a on which is formed the floating gate 13
30 and the select gate 14. Overlying floating gate 13 is insulation 16b, typically a composition layer of thermally grown oxide, deposited silicon nitride, and thermally grown oxide and nitride. A control gate 17 is formed on top of the insulation 16b. Typically both the
35 floating gate 13 and the control gate 17 are formed of polysilicon. An insulation 16c is formed on the sidewall

of the floating gate 13 and the control gate 17. The select gate 14 is formed by depositing the third layer of polysilicon and then by etching back the polysilicon to form a polysilicon spacer. The programming (high threshold voltage) of the cell is accomplished by raising the control gate to about 17 volts, the select gate to slightly above the threshold voltage of the select gate transistor which is about 1.5 volts, the drain to 5 volts, and the source to ground. The channel electrons are accelerated through a potential drop in between the select gate and the floating gate transistors. It is known that the hot electron injection efficiency using this method can be a thousand times higher than the conventional lateral acceleration method. Due to the high programming efficiency, the flash cell can be programmed with a lower drain voltage (5 volts) and with very low programming current (few micro-amperes). Erase of the cell is achieved by raising the drain region 11b to 14 volts, grounding the control gate, and opening the source (floating). The high erase voltage can be obtained by using a charge pump technique from a 5 volt power supply. These features allow operation with a single 5 volt power supply.

Several major drawbacks in the prior art flash EEPROM of FIG. 1 relates to the formation of the select gate transistor. First, the split gate cell as disclosed in the prior art consists of two transistors which are the floating gate and the select gate. It takes the space of two transistors to form a single memory bit when it is implemented in a memory array. This is a common drawback for conventional split gate structure and imposes a major limitation for implementing a high density memory array. Second, the select gate is a polysilicon spacer which is formed by the polysilicon etching-back technique, and the length of the select gate is determined by the combined height of the floating gate

and the control gate which is about 0.4 μm . Punchthrough of this transistor is very difficult to prevent with this small channel length, especially when the floating gate is over erased to a negative threshold. Third, the select gate is formed of polysilicon and it is very difficult to apply deposited polycide on a polysilicon spacer. Thus, in the prior art, only polysilicon with resistance around 20 to 30 ohm per square can be used for the select gate. As a result, the word line RC delay of a memory circuit is considerably longer than in the conventional memory circuit in which the polycide with resistance in the range of 2 to 4 ohm per square is used. Fourth, due to the etching-back method in the prior art, the select gate can only run parallel to the control gate. However, in a high density virtual ground array the select gate must be perpendicular to the control gate. Thus, the flash EEPROM cell in the prior art FIG. 1 cannot be implemented in a higher density virtual ground array structure.

As disclosed in our co-pending application serial no. 07/585,811 filed September 20, 1990 for "Triple Polysilicon Flash EPROM Device," a conventional virtual ground memory array as shown in FIG. 1B is formed by using the flash EPROM cell as disclosed in the above application. The channel length of the select gate transistor is non-self-aligned and is defined by using a photoresist as a bit line mask as shown in FIG. 1C. Due to the mis-alignment between the bit line mask and the stacked floating and control gates, the non-self-aligned select gate channel length is determined by the photoresist to floating gate edge dimension 19B and the mis-alignment tolerance (MA). Typically, the mis-alignment tolerance is in the range of 0.3 to 0.5 μm which will be a major limitation for high density memory array. As shown in FIG. 1B, since each memory bit needs one bit line diffusion 18, one floating gate length 19A,

and one non-self-align select gate length $19B + MA$, the total dimension per memory bit is equal to $18 + 19A + 19B + MA$. It can be seen that in the conventional split gate virtual ground array as shown in FIG. 1B, each floating gate transistor needs one select gate transistor in which the select gate transistor is non-self-aligned to the floating gate edge. This indicates that the convention split gate virtual ground may have its limitation for implementing an ultra high density memory array.

SUMMARY OF THE INVENTION

An object of the invention is a dual-bit split gate flash EEPROM cell structure using one select gate transistor and two floating gate transistors to form two memory bits in one cell.

Another object of the invention is a method of making a fully self-aligned split gate flash EEPROM cell structure by using self-aligned etching step to accurately define the channel length of the select gate transistor.

Still another object of the invention is a high density dual-bit flash EEPROM array using the dual-bit split gate flash EEPROM cell.

A feature of the invention is that in the dual-bit split gate flash EEPROM cell, a single select gate transistor is shared by two adjacent floating gate transistors, i.e., a single select gate transistor is used for two memory bits.

Another feature of the invention is that dual-bit split gate flash EEPROM cell, the select gate transistor in the split gate structure is fully self-aligned.

Still another feature is that in the dual-bit flash EEPROM array, two floating gate transistors are put in-between two bit lines.

Still another feature of the invention is that in the dual-bit flash EEPROM cell, the access of one of the two floating gate transistors is through the turn-on of the select gate transistor and the other floating gate transistor.

Another feature of the invention is that the select transistor in the split gate structure is fully self-aligned.

The present invention relates to a high density flash EEPROM cell which is made by a triple-polysilicon process with a split gate structure and four terminals (control gate, select gate, drain and source) wherein one select gate transistor is shared by two floating gate transistors. Unlike the split gate structure disclosed in the prior art and the conventional split gate virtual ground array as disclosed in the co-pending application in which each floating gate transistor needs one select gate transistor the dual-bit split gate cell needs only half of the select gate transistor for each floating gate transistor. Moreover, unlike the conventional split gate cell in which the channel length of the select gate transistor is non-self-aligned to the edge of the floating gate transistor, the channel length of the select gate transistor in the dual-bit split gate cell is accurately defined and is fully self-aligned by the separation of two floating gate transistors which is formed by self-aligned polysilicon etching step.

In a preferred embodiment a high density 5 volt virtual ground flash EEPROM cell is fabricated using the triple polysilicon process with a split gate structure and the four terminals (control gate, select gate, drain and source) for each cell. One select transistor is shared by two floating gate transistor cells. The channel length of the select transistor is fully aligned with the floating gate transistors and is defined in a self-alignment etching process in forming the control

gate and floating gate for each of the two floating gate transistors.

Advantageously, the select gate runs perpendicular to the bit lines as required in a virtual ground flash EEPROM. The select gate can have a polycide layer formed thereon to reduce resistance and RC delay of a word line.

The invention and objects and features thereof will be more readily apparent from the following detailed description and appended claims when taken with the drawings.

The invention and objects and features thereof will be more readily apparent from the following detailed description and appended claims when taken with the drawings.

BRIEF DESCRIPTION OF THE DRAWING

FIGURE 1A is a section view of a triple polysilicon EEPROM cell in accordance with the prior art, and FIGURES 1B and 1C are section views of a triple polysilicon flash EPROM device in accordance with our co-pending application

FIGURE 2A, 2B, and 2C are a section view, plan view, and electrical schematic of a triple polysilicon EEPROM cell in accordance with one embodiment of the present invention.

FIGURE 3 is plan view of a portion of a memory array using the EEPROM cells of FIGS. 2A-2C.

FIGURES 4A-4C are section view illustrating steps in fabricating the cell structure of FIGS. 2A-2C.

FIGURE 5A is a plot of transistor threshold voltage versus programming time for the two cell structure of the invention.

FIGURE 5B is a plot of threshold voltage versus select gate voltage in programming the cell structure of the invention.

FIGURE 6 is a plot of control gate voltage versus read current for the cell structure of the invention.

FIGURE 7 is a plot of transistor threshold voltage versus erase time in erasing a cell of the structure of the invention.

DETAILED DESCRIPTION OF THE ILLUSTRATIVE EMBODIMENTS

Referring now to the drawings, FIGS. 2A, 2B, and 2C are a section view, top plan view, and schematic of a dual-bit flash EEPROM cell in accordance with one embodiment of the invention. The cell structure comprises a first floating gate storage transistor 20, a second floating gate storage transistor 22, and a select gate transistor 24 which serially connects transistors 20, 22. As illustrated schematically in FIG. 2C, a first bit line BL1 is connected to the drain of transistor 20, a second bit line BL2 is connected the drain of transistor 22, and the sources of the two transistors are serially connected through the select gate 24. As will be described further herein below, when reading storage transistor 20, transistors 22 and 24 are turned on and the drain of transistor 22 in effect becomes the source of transistor 20. Conversely, when reading transistor 22, transistors 20 and 24 are turned on and the drain of transistor 20 effectively becomes the source of transistor 22.

Referring to the section view of FIG. 2A, the cell structure is formed in a P- doped substrate 26 with the drain 20a of transistor 20 and the drain 22a of transistor 22 comprising N+/N- doped regions in the surface of the substrate 26. The drains are interconnected with drains in common rows of transistors and form the cell bit lines. Transistor 20 includes a floating gate 20b and an overlying control gate 20c with the floating gate 20b separated from the surface of

substrate 26 by a thin (e.g. 100 angstrom) gate oxide 20d, and the control gate 20c separated from the floating gate 20b by a dielectric 20e which can comprise silicon oxide, silicon nitride, or combination thereof.

5 Similarly, transistor 22 includes a floating gate 22b, a control gate 22c, with dielectrics 22d and 22e electrically isolating the floating gate and control gate from each other and from the substrate. Dielectric 20f and 22f form part of a dielectric layer overlying the
10 control gates and the surface of substrate 26. A word line 28 extends over the dielectric layer and forms the control gate 24a of the select transistor intermediate the floating gate transistors 20, 22. The word line 28 serially connects the gates of the select transistors in
15 one row of a memory array and runs perpendicular to the bit lines connected to the drains of transistors in columns such as drains 20a and 22a as illustrated in the plan view of a portion of a flash EEPROM array shown in FIG. 3.

20 FIG. 2A shows the section view of the present invention in which a dual-bit split gate flash EEPROM cell contains two memory bits. Unlike the split gate structure disclosed in the prior art and the conventional split gate virtual ground array as disclosed in the co-
25 pending application in which each floating gate transistor needs one select gate transistor the dual-bit split gate cell needs only half of the select gate transistor for each floating gate transistor. Moreover, unlike the conventional split gate cell in which the
30 channel length of the select gate transistor is non-self-aligned to the edge of the floating gate transistor, the channel length of the select gate transistor in the dual-bit split gate cell is accurately defined and is fully self-aligned by the separation of two floating gate
35 transistors which is formed by self-aligned polysilicon etching step. As shown in FIG. 2A, each memory bit

consists of one half of diffusion 20A, one floating gate length 20G, and one half of the select gate length 24G such that the total dimension of one memory bit is equal to half of 20A + 20G + half of 24G. The half select gate for each memory bit and the fully self-alignment of the select gate channel length features make the dual-bit split gate most scaleable for ultra high density memory array in the application such as solid-state-disk-drive and IC memory card. In addition, when compared to the prior art, the select gate can be implemented by using polycide to reduce the work line RC delay.

Fabrication of the cell structure of FIGS. 2A-2C is illustrated in the section views of FIGS. 4A-4C. Like elements have the same reference numeral. First a thin gate oxide of approximately 100 angstroms is thermally grown on the surface of P- doped semiconductor substrate 26 having a resistivity of 10-25 ohm-centimeter. A first layer of doped polysilicon is then deposited on top of the thin oxide and is patterned in one direction to partially form the floating gate layer. An insulation layer of silicon oxide, silicon nitride, or combination thereof is then formed on top of the floating gate layer, and a second doped polysilicon layer is then deposited and patterned in one direction for the control gates. In so doing, the double polysilicon stack is etched to form the control gates 20c, 22c and the floating gates 20b, 22b which are self-aligned, as indicated, with insulation therebetween. Similar structures are formed for adjacent transistors are illustrated at 30 and 32.

Next, as illustrated in FIG. 4B a photoresist layer 34 is formed and patterned to partially cover one portion of the double polysilicon stack, and an ion implantation step forms the bit line regions 20a and 22a. By implanting two different n-type dopants such as arsenic and phosphorous and then annealing the structure,

the N+/N- dopant profile results. This process is described in co-pending application serial no. 07/585,811, supra. The substrate region which is covered by the photoresist between the stacked control
5 gate/floating gate structure does not receive the ion implantation and is used to define the channel length of the select gate transistor.

The photoresist is stripped, and a silicon oxide insulation layer is formed on the top and side
10 walls of the double polysilicon stacks. A third layer of doped polysilicon is then deposited and patterned to form a word line and the select gate 24 as shown in FIG. 4C. The word line is perpendicular to the control gates and runs to adjacent select gates along the word line. The
15 select gate is accurately defined by the separation of the two floating gate transistors which are formed by the self-aligned etching step. The channel length of the select transistor is about 0.6 to 0.8 micron and is fully aligned with the floating gate transistors. Note that
20 the select transistor channel 24g is positioned between the channels 20g and 22g of the floating gate transistor 20 and 22, respectively, as shown in FIGS. 2A. A polycide coating can be applied on the select gate and word line to reduce the word line RC delay. Moreover, by
25 running the select gate perpendicular to the control gate the flash EEPROM cell can be implemented in a high density virtual ground array.

Programming of the floating gate transistor 20 is achieved by raising the control gates 20c and 22c to
30 12 volts, the select gate 24a to slightly above the threshold voltage of the select gate transistor (approximately 2 volts) the bit line (drain) 20a to 5 volts, and the bit line (drain) 22a is grounded. The floating gate transistors are fully turned on due to the
35 12 volts on the control gates and the select gate transistor being slightly turned on. Under this

condition channel current during programming is controlled by the select gate transistor and is in the range of 10-20 microamps. The channel electrons are accelerated at the potential drop between the select gate region 24g and the floating gate region 20a and are injected into the floating gate 20b through the barrier of the thin gate oxide 20d by hot electron injection.

A read operation of the floating gate transistor 20 is achieved by putting 12 volts on the control gate of transistor 22 to turn on the transistor 22, 5 volts on select gate 24 and control gate 20c, 1-2 volts on bit line 20a, and grounding bit line 22a. The back bias effect from floating gate transistor 22 is about 0.17 to 0.24 volt when its threshold voltage is -0.25 and 6.6 respectively.

The erase operation of the floating gate transistor 20 is achieved by raising the bit line 20a to 12 volts, grounding the control gates 20c and 22c, and opening the bit line 22a. Electrons are discharged from the floating gate 20b to the bit line 20a through Fowler-Nordheim tunneling effect.

The read, program, and erase operation conditions of the flash EEPROM cell are summarized in the following table:

	<u>READ CELL 1</u>	<u>PROGRAM CELL 1</u>	<u>ERASE CELL 1</u>
	V _{sg} 5	1.8 ~ 2	0
	V _{cg1} 5	12	0
	V _{cg2} 12	12	0
	V _{BL1} 1 ~ 2	5	12
	V _{BL2} 0	0	floating

Note that the above table assumes that the cell is working with a 5 volt power source. A charge pump is required to generate the 12 volts necessary for programming, reading, and erasing the cell. However, if

a 12 volt source is available the use of a charge pump is obviated, and the voltage on bit line 1 during programming can be increased to 6.5 volts to increase the speed of programming.

5 FIG. 5A is a plot illustrating threshold voltage change during programming versus programming time, and it will be noted that the threshold voltage of a transistor can be changed by more than 4.5 volts in less than 10 micro seconds. FIG. 5B is a plot illustrating the effect
10 of select gate voltage, VSG on the programming of one floating gate transistor using 10 microsecond pulses. It can be seen that there is very little difference when the other floating gate transistor is at a high or low threshold voltage state.

15 FIG. 6 is a plot of control gate voltage versus the read current when the floating gate transistors are at a high or low threshold voltage state.

 FIG. 7 is a plot illustrating erase time versus threshold voltage for a transistor during an erase
20 operation. The cell can be erased to zero threshold voltage in about 100 milliseconds.

 There has been described a novel dual-bit flash EEPROM cell structure in which a pair of floating gate storage transistors share a single select gate
25 transistor. The word lines interconnecting the select gates run perpendicular to the control gate lines and the bit lines interconnecting the drains of the floating gate transistors thus permitting a virtual ground flash array. Further, the word lines can have a silicide coating thus
30 reducing the resistance and RC delay associated with the word lines. Unlike the spacer select gate of the prior art, the channel length of the select gate transistor is readily defined by the self-aligned etch of the floating gate transistors thus facilitating the optimization of
35 the punch through characteristics of the select gate transistor. The fully self-aligned structure of the

select transistor makes this cell the most scaleable in split gate structures.

5 While the invention has been described with reference to specific embodiments, the description is illustrative of the invention and is not to be construed as limiting the invention. Various modifications and applications may occur to those skilled in the art without departing from the true spirit and scope of the invention as defined by the appended claims.

WHAT IS CLAIMED IS:

1. A dual-bit flash EEPROM cell structure comprising a semiconductor substrate having a surface region of one conductivity type,

5 a first drain region and a second drain region formed in said surface region, said drain regions being of second conductivity type opposite from said one conductivity type,

10 a first stacked floating gate and control gate and a second stacked floating gate and control gate on said surface region between said first drain region and said second drain region, said first and second stacked floating gate and control gate being spaced apart,

15 a select gate on said surface region between said first and second stacked floating gate and control gate,

a first bit line contacting said first drain region,

a second bit line contacting said second drain region, and

20 a word line contacting said select gate, said word line being oriented generally perpendicular to said first bit line and said second bit line.

2. The dual-bit flash EEPROM cell structure as defined by claim 1 wherein said select gate transistor is shared by said first and second stacked floating gate and control gate.

3. The dual-bit flash EEPROM cell structure as defined by claim 1 wherein the access of said first floating gate transistor is through the turn-on of said select gate and said second floating gate transistors.

4. The dual-bit flash EEPROM cell structure as defined by claim 1 wherein the channel of said select

gate transistor is self-aligned with said first stacked floating gate and control gate and said second stacked floating gate and control gate.

5. The dual-bit flash EEPROM cell structure as defined by claim 1 wherein said floating gates are formed from a first polysilicon layer, said control gates are formed from a second polysilicon layer, and said select gate is formed from a third polysilicon layer.

6. The dual-bit flash EEPROM cell structure as defined by claim 5 wherein said word line includes a layer of polycide.

7. The dual-bit flash EEPROM cell structure as defined by claim 5 and further including a first dielectric layer formed on said surface region and separating said first floating gate and said second floating gate from said substrate, a second dielectric layer on said floating gates and separating said control gates from said floating gates, and a third dielectric layer on said control gates and said substrate between said first and second stacked floating gate and control gate, said third dielectric layer separating said word line and said select gate from said substrate.

8. The dual-bit flash EEPROM cell structure as defined by claim 1 wherein programming, reading, and erasing a floating gate transistor is accomplished according to the following table:

<u>READ CELL 1</u>	<u>PROGRAM CELL 1</u>	<u>ERASE CELL 1</u>
V _{sg} 5	1.8 ~ 2	0
V _{cg1} 5	12	0
V _{cg2} 12	12	0
V _{BL1} 1 ~ 2	5	12
V _{BL2} 0	0	floating

where V_{sg} is the voltage applied to said select gate,
 V_{cg1} is the voltage applied to a first control gate,
15 V_{cg2} is the voltage applied to a second control gate,
 V_{BL1} is the voltage applied to said first bit line,
 V_{BL2} is the voltage applied to said second bit line.

9. A flash EEPROM array comprising
a plurality of dual-bit flash EEPROM cell structures arranged in rows and columns, each cell structure including first and second floating gate transistors separated by a select gate transistor,
5 a plurality of bit lines interconnecting drains of floating gate transistors of cell structures aligned vertically,
a plurality of word lines interconnecting select gates of cell structures aligned horizontally,
10 floating gates of said floating gate transistors being formed from a first polysilicon layer, the control gates of all floating gate transistors being formed from a second polysilicon layer, and said word lines and said
15 select gates being formed from a third polysilicon layer.

10. The flash EEPROM array as defined by claim 9 wherein two bits are stored between adjacent bit lines.

11. The dual-bit flash EEPROM array as defined by claim 9 wherein programming, reading, and erasing a floating gate transistor in a cell structure is accomplished according to the following table:

5	<u>READ CELL 1</u>	<u>PROGRAM CELL 1</u>	<u>ERASE CELL 1</u>
	V _{sg} 5	1.8 ~ 2	0
	V _{cg1} 5	12	0
	V _{cg2} 12	12	0
	V _{BL1} 1 ~ 2	5	12
10	V _{BL2} 0	0	floating

where

V_{sg} is the voltage applied to said select gate,

V_{cg1} is the voltage applied to a first control gate,

15 V_{cg2} is the voltage applied to a second control gate,

V_{BL1} is the voltage applied to said first bit line,

V_{BL2} is the voltage applied to said second bit line.

12. A method of fabricating a flash EEPROM cell structure comprising the steps of

a) providing a semiconductor substrate having a surface region of a first conductivity type,

5 b) forming a first dielectric layer on said surface region,

c) forming a first doped polysilicon layer on said first dielectric layer,

10 d) selectively etching said first doped polysilicon layer,

e) forming a second dielectric layer on said first doped polysilicon layer,

f) forming a second doped polysilicon layer on said second dielectric layer,

15 g) selectively etching said second doped polysilicon layer, said second dielectric layer, said first doped polysilicon layer, and said first dielectric layer to form a first and a second stacked control gate

and floating gate from said second doped polysilicon layer and said first doped polysilicon layer, said first or second stacked control gate and floating gate being spaced apart,

h) selectively implanting dopant of a second conductivity type opposite from said first conductivity type into said surface region using photoresist and said first and second stacked control gate and floating gate as a mask, said dopant forming first and second drains for first and second floating gate transistors, each of said drains being self-aligned with one of said stacked control gate and floating gate,

i) forming a third dielectric layer over said control gates and on said substrate between said first and second stacked control gate and floating gate,

j) forming third doped polysilicon layer over said third dielectric layer, and

k) selecting etching said third doped polysilicon layer to form a word line over said first and second stacked control gate and floating gate and between said first and second stacked control gate and floating gate.

13. The method as defined by claim 12 wherein step g) defines the channel of a select transistor which is self-aligned with said first and second stacked control gate and floating gate.

14. The method as defined by claim 12 wherein step j) further includes forming a polycide layer on said word line.

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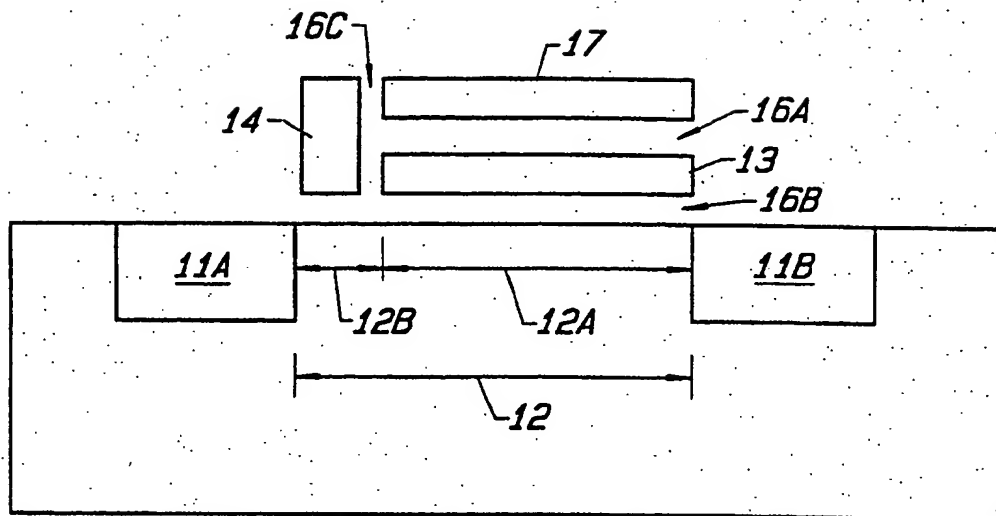


FIG. 1A
PRIOR ART

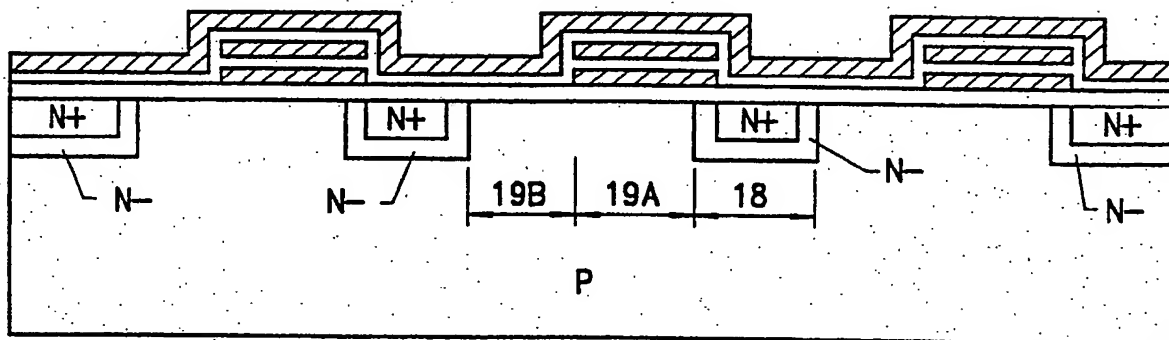


FIG. 1B

BITLINE RESIST

BITLINE RESIST

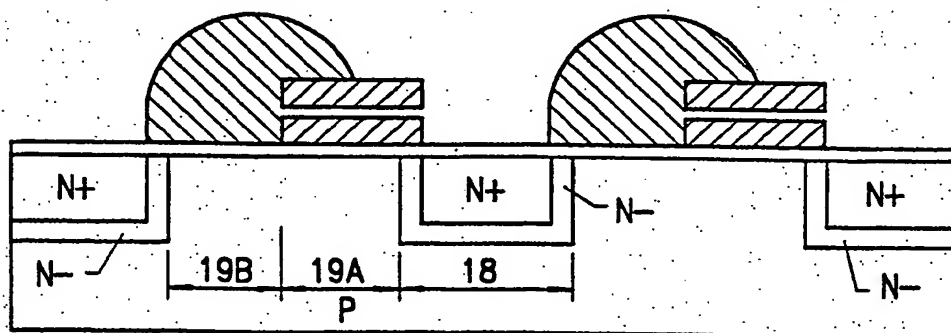


FIG. 1C

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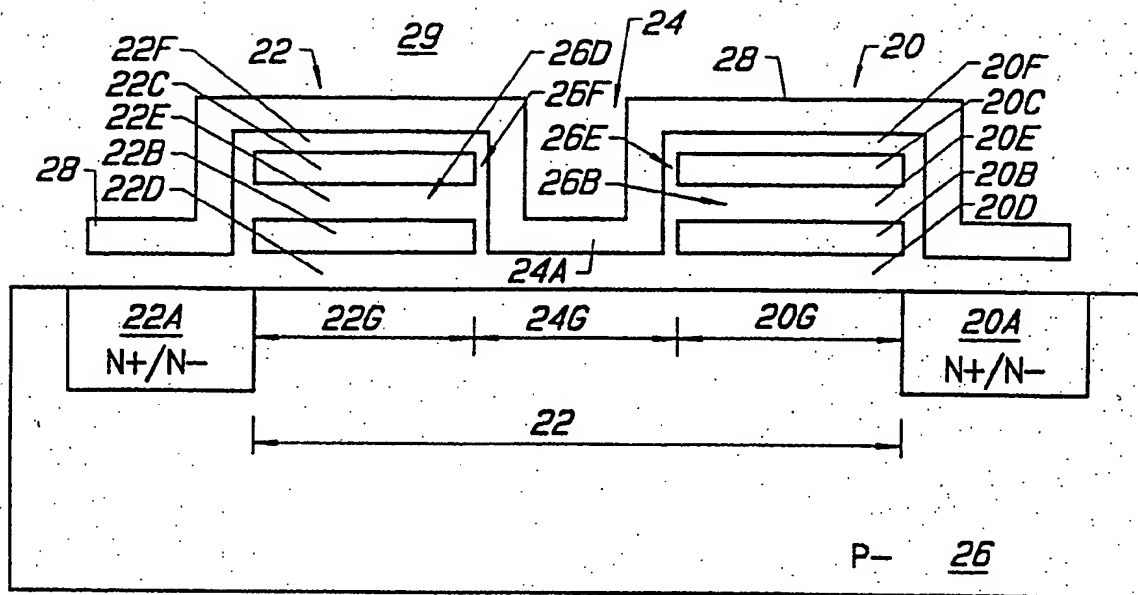


FIG. 2A

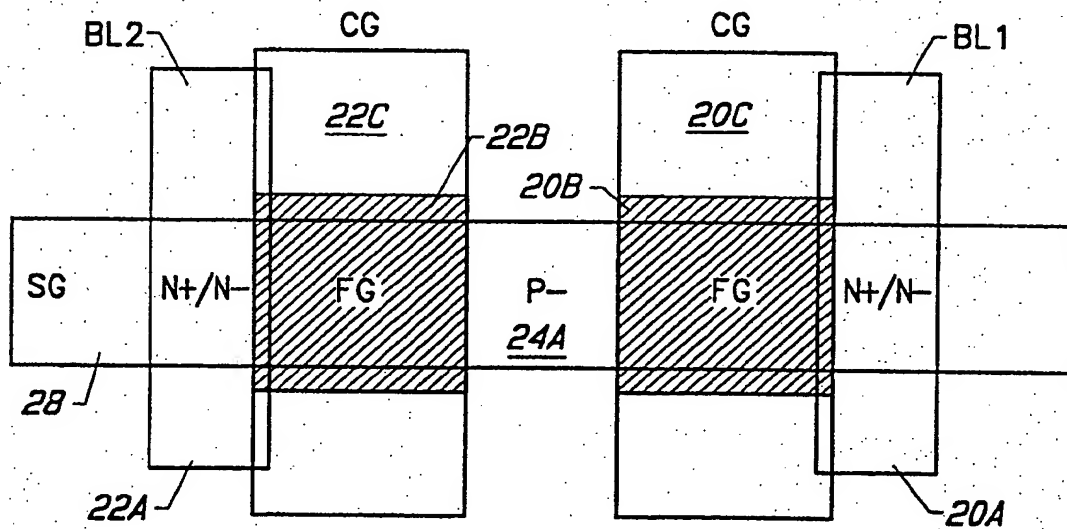


FIG. 2B

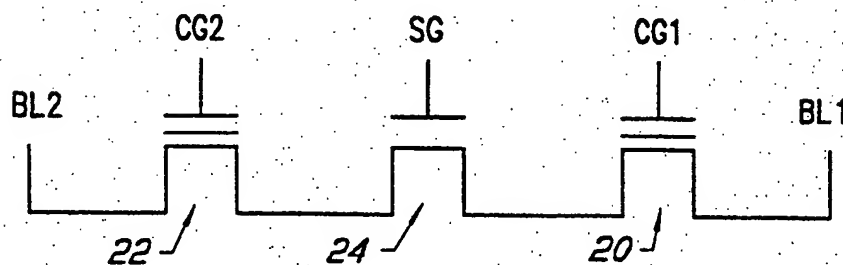


FIG. 2C

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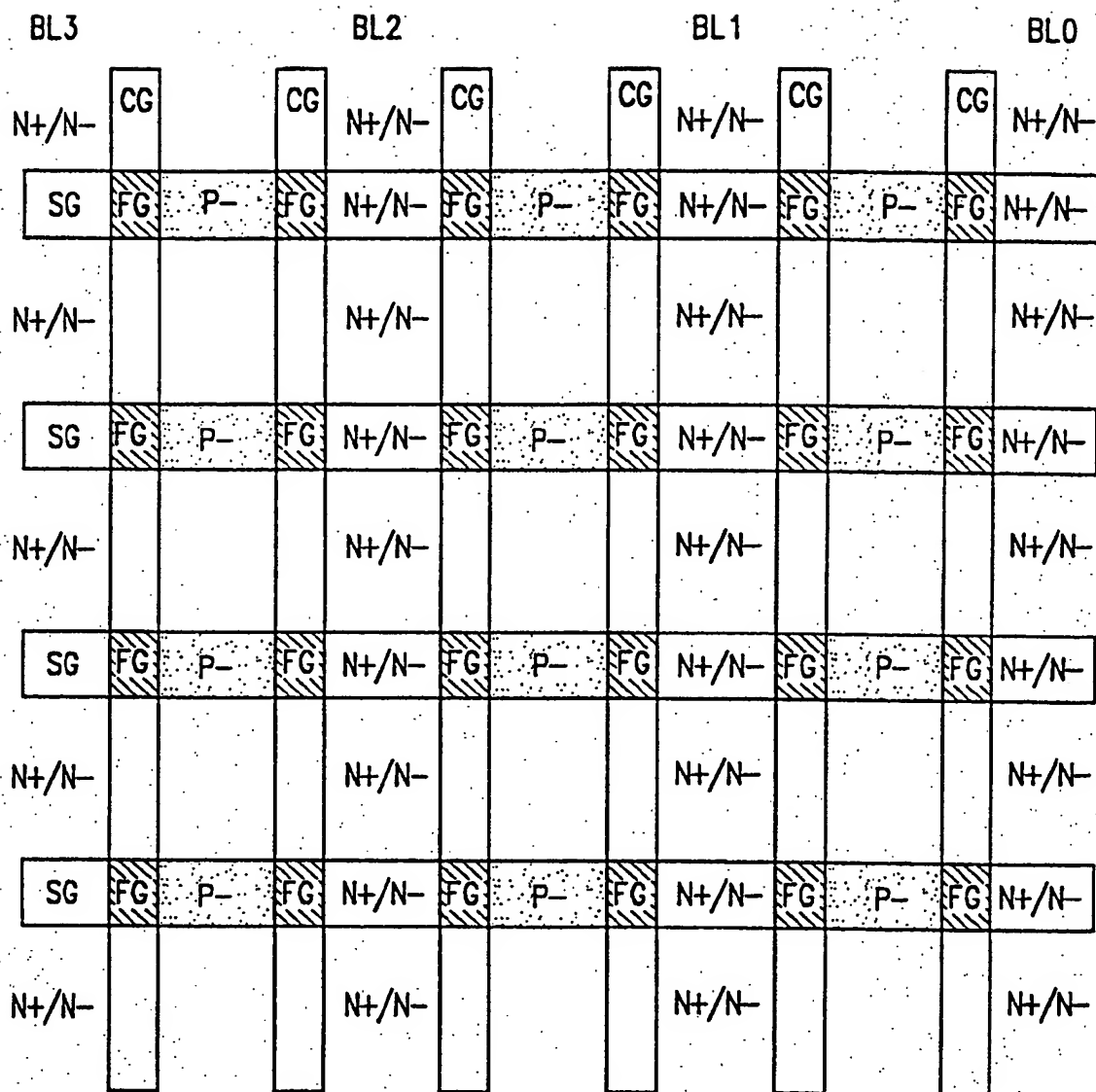


FIG. 3

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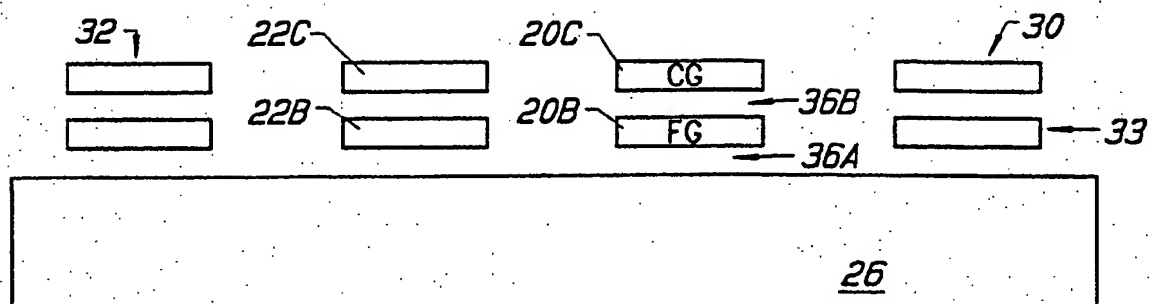


FIG. 4A

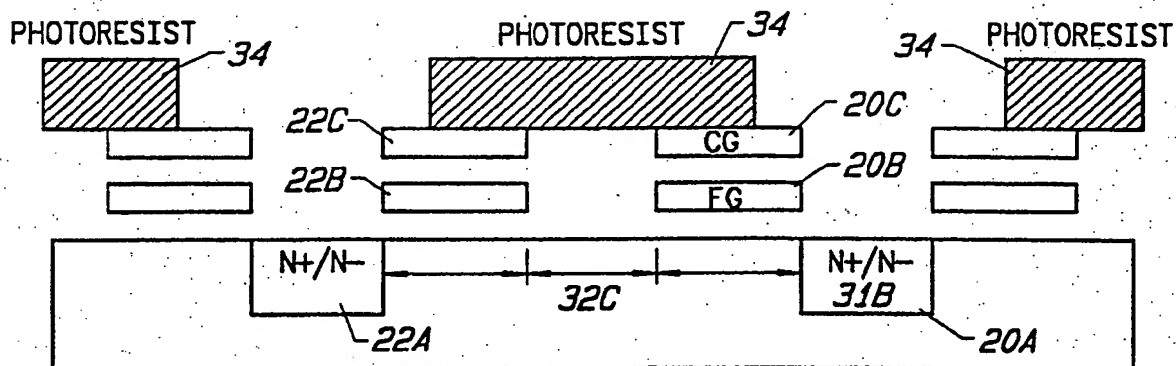


FIG. 4B

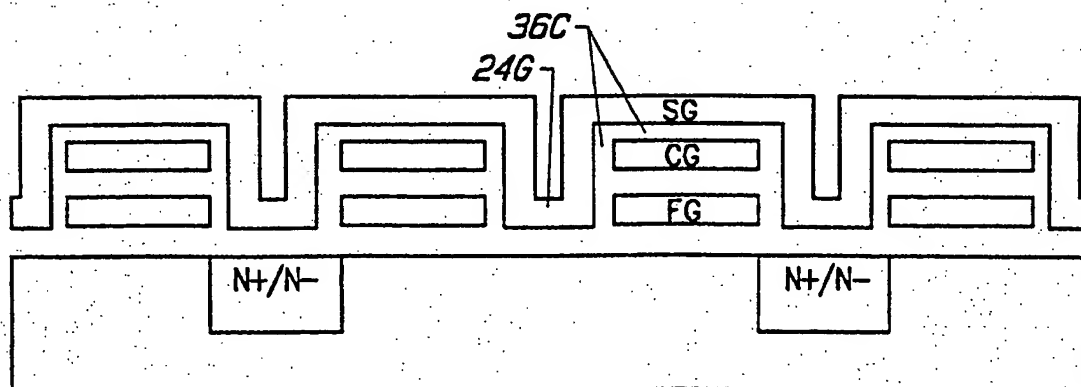


FIG. 4C

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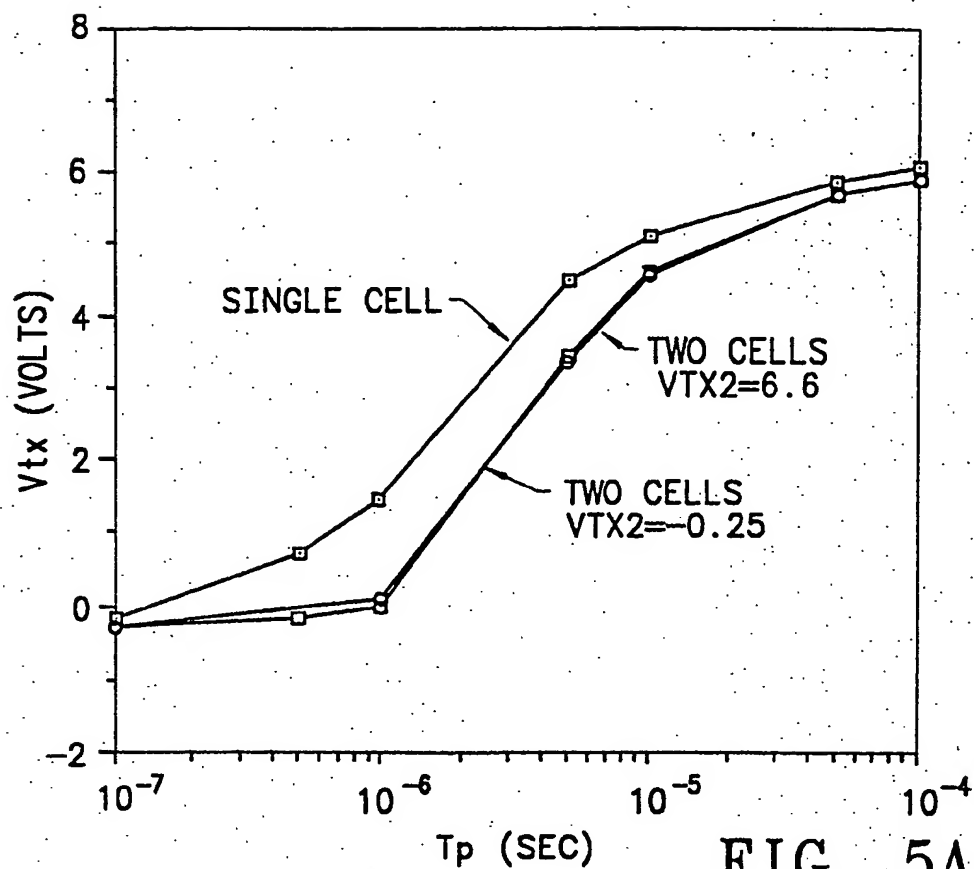


FIG. 5A

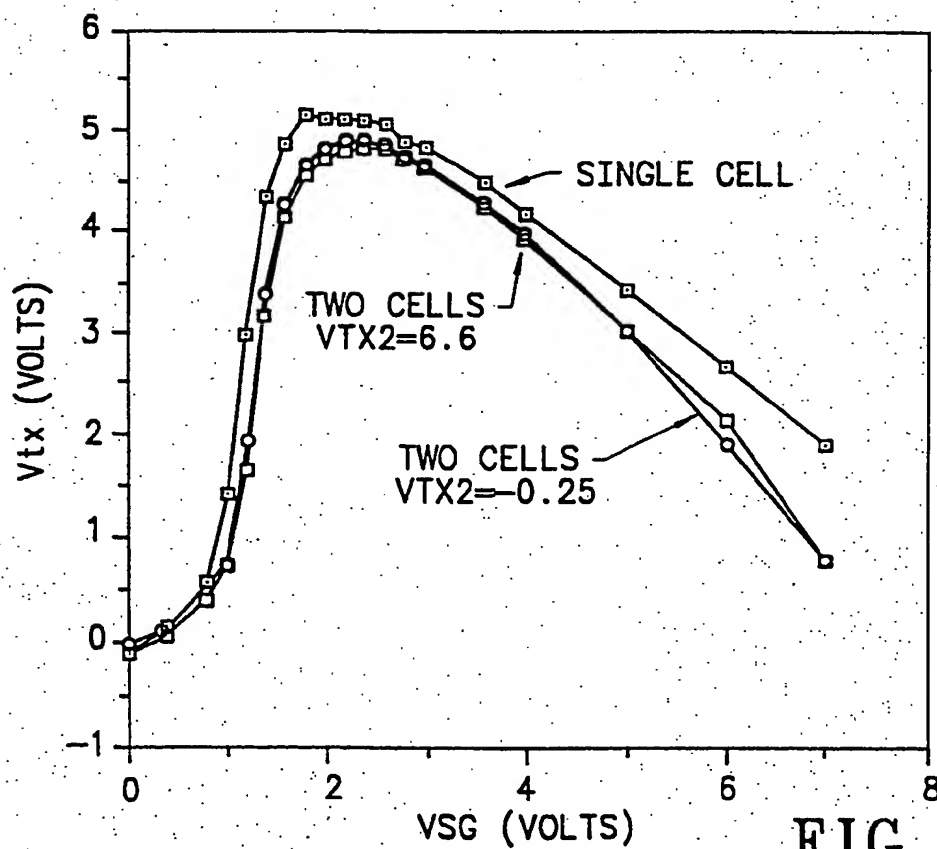


FIG. 5B

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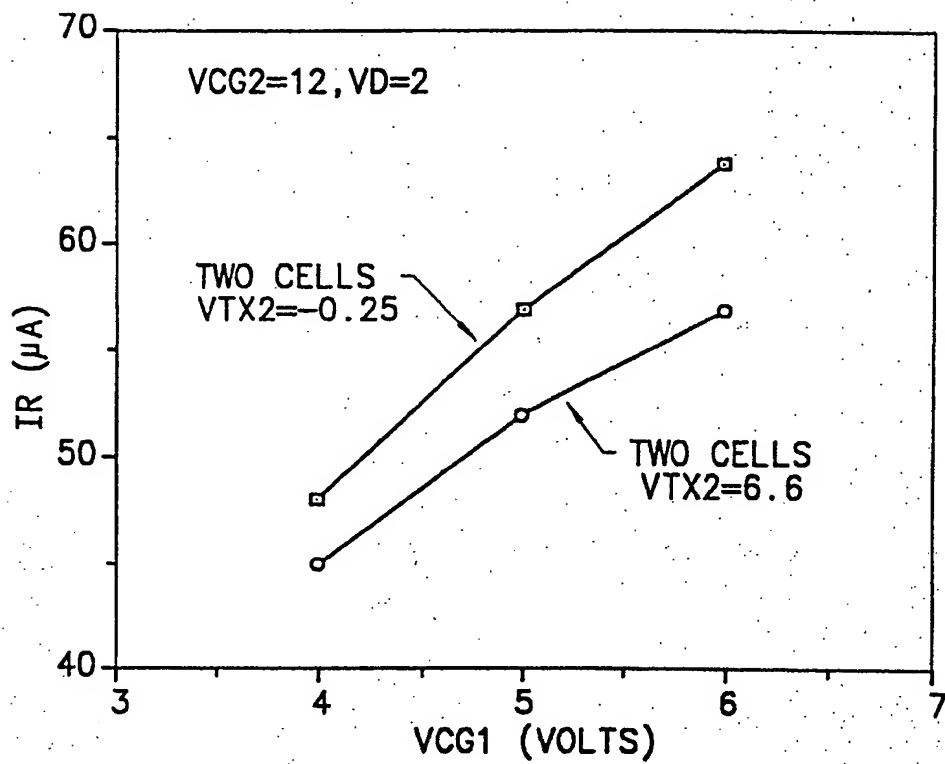


FIG. 6

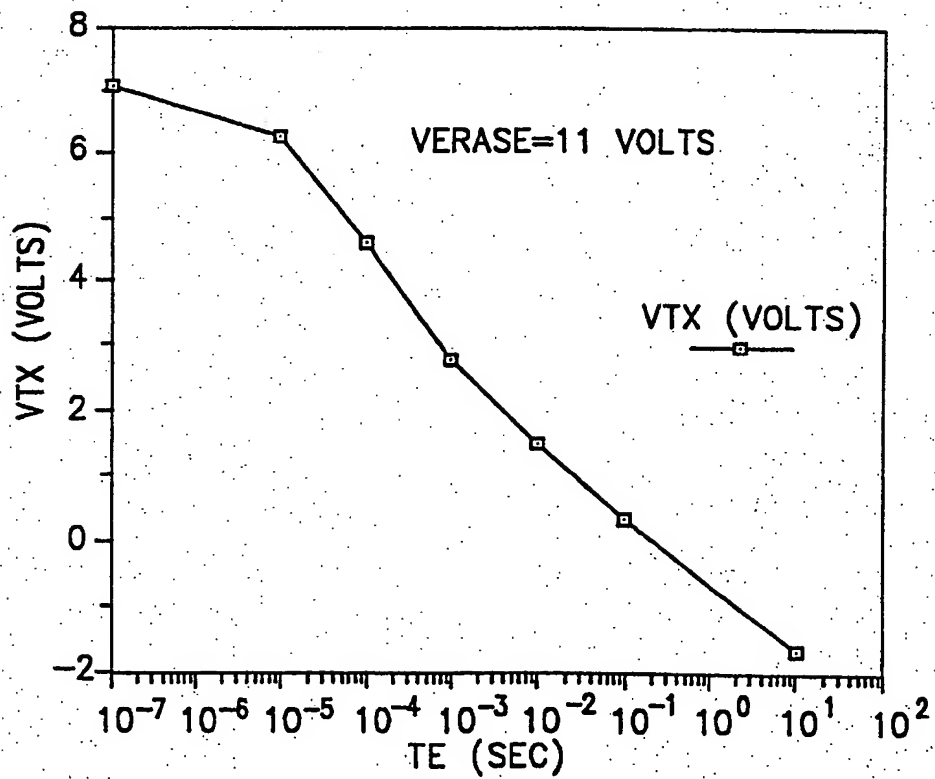


FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/00407

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) : H01L 29/68, 29/78

US CL : 257/319, 315, 316; 365/185; 437/48, 49

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/319, 315, 316, 317, 319, 321; 365/185; 437/47, 48, 49

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
E	US, A, 5.278,439 (Ma et al.) 11 January 1994, entire document.	1-14
Y	JP, A, 58-222561 (Harada) 24 December 1983, figure 2.	9 and 10
A	JP, A, 62-14473 (Hayashi) 23 January 1987, see figure 1c.	1, 9 & 10
A	US, A, 4,417,264 (Angle) 22 November 1983, cols. 3 and 4.	8, 12 & 13



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:	*T*	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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L document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	*Z*	document member of the same patent family
O document referring to an oral disclosure, use, exhibition or other means		
P document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search

04 April 1994

Date of mailing of the international search report

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